```
#PACE: Start of Constraints generated by PACE

#PACE: Start of PACE I/O Pin Assignments
NET "START" IOSTANDARD = LVCMOS33 ;
NET "STOP" IOSTANDARD = LVCMOS33 ;
NET "CLK" IOSTANDARD = LVCMOS33 ;
NET "RESET" IOSTANDARD = LVCMOS33 ;
NET "START_S1B" IOSTANDARD = LVCMOS33 ;
NET "START_S2B" IOSTANDARD = LVCMOS33 ;
NET "START_S3B" IOSTANDARD = LVCMOS33 ;
NET "STOP_S1B" IOSTANDARD = LVCMOS33 ;
NET "STOP_S3B" IOSTANDARD = LVCMOS33 ;
NET "DOUT*" IOSTANDARD = LVCMOS33 ;
NET "CEO" IOSTANDARD = LVCMOS33 ;
NET "TC" IOSTANDARD = LVCMOS33 ;

#PACE: make inputs schmitt triggered (for slow transitions)
NET "START" SCHMITT_TRIGGER;
NET "STOP" SCHMITT_TRIGGER;
NET "RESET" SCHMITT_TRIGGER;

#PACE: make output pins slew-rate limited (2 ns instead of 1 ns?)
NET "START_S1B" SLOW;
NET "START_S2B" SLOW;
NET "START_S3B" SLOW;
NET "STOP_S1B" SLOW;
NET "STOP_S3B" SLOW;
NET "DOUT*" SLOW;
NET "CEO" SLOW;
NET "TC" SLOW;

#PACE: Start of PACE Area Constraints

NET "CLK" LOC = PIN1;      # main high-frequency clock signal

#PACE: Start of PACE Prohibit Constraints

#PACE: End of Constraints generated by PACE

```