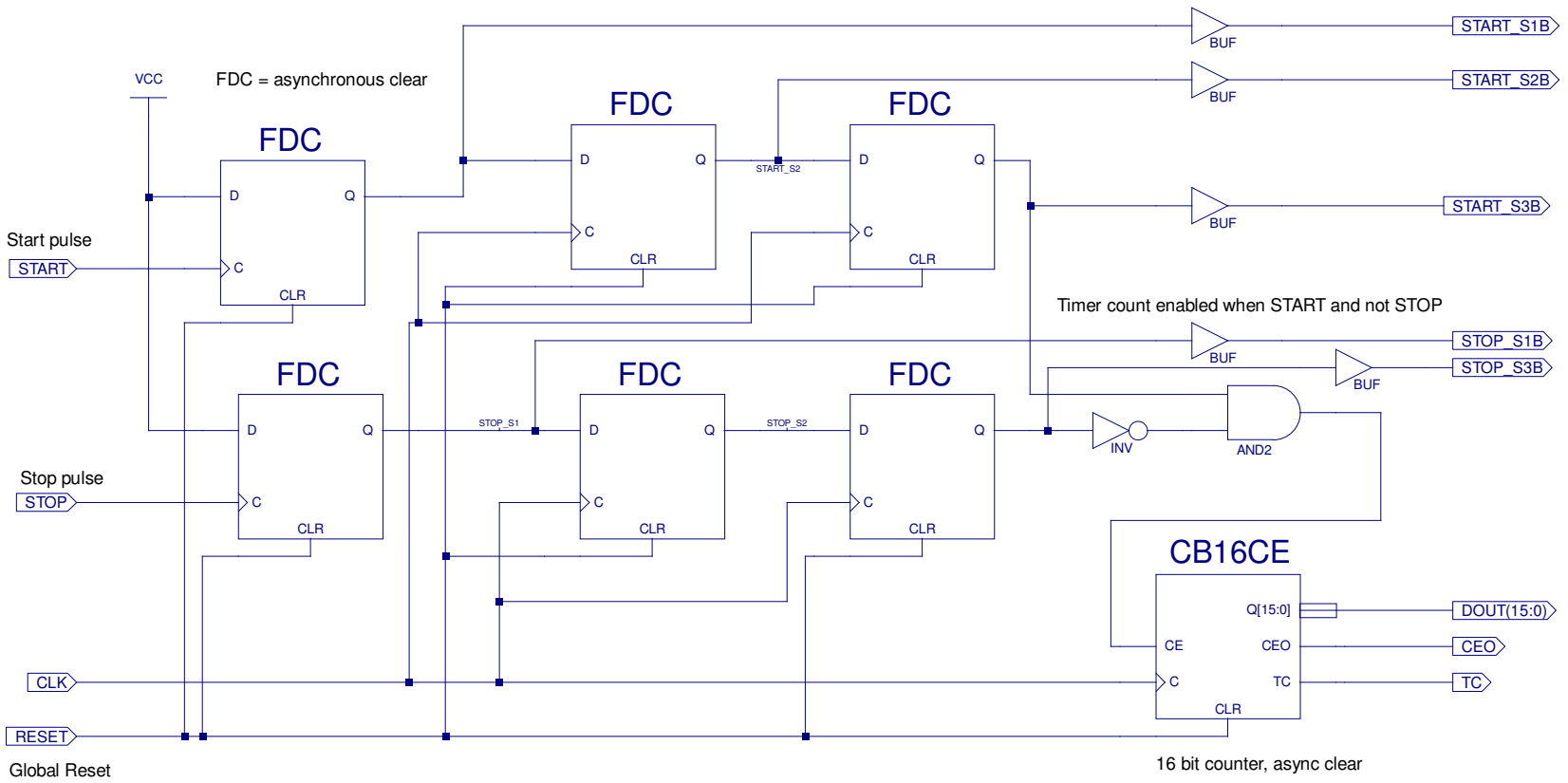
Two-stage synchronizer for START and STOP pulses



16-bit counter with START and STOP pulse input for Coolrunner-II CPLD

John Beale Dec 17 2011