Timing Report

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Design Name	c3schem
Device, Speed (SpeedFile Version)	XC2C64A, -7 (14.0 Advance Product Specification)
Date Created	Sun Apr 10 20:47:49 2011
Created By	Timing Report Generator: version O.40d
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Summary

Notes and Warnings
Note: This design contains no timing constraints.
Note: A default set of constraints using a delay of 0.000ns will be used for analysis.

Performance Summary	
Min. Clock Period	6.300 ns.
Max. Clock Frequency (fSYSTEM)	158.730 MHz.
Limited by Cycle Time for CLK	
Clock to Setup (tCYC)	6.300 ns.
Setup to Clock at the Pad (tSU)	2.500 ns.
Clock Pad to Output Pad Delay (tCO)	17.000 ns.

Timing Constraints

Constraint Name	Requirement (ns)	Delay (ns)	Paths	Paths Failing
TS1000	0.0	0.0	0	0
TS1001	0.0	0.0	0	0
TS1002	0.0	0.0	0	0
AUTO_TS_F2F	0.0	6.3	156	156
AUTO_TS_P2P	0.0	17.0	19	19
AUTO_TS_P2F	0.0	5.6	9	9

AUTO_TS_F2P	0.0	13.9	51	51

Constraint: TS1000

Description: PERIOD:PERIOD_START:0.000 nS

Path	Requirement (ns)	Delay (ns)	Slack (ns)

Constraint: TS1001

Description: PERIOD:PERIOD_STOP:0.000 nS

Path	Requirement (ns)	Delay (ns)	Slack (ns)

Constraint: TS1002

Description: PERIOD:PERIOD_CLK:0.000 nS

Path	Requirement (ns)	Delay (ns)	Slack (ns)

Constraint: AUTO_TS_F2F

Description: MAXDELAY:FROM:FFS(*):TO:FFS(*):0.000 nS

Path	Requirement (ns)	Delay (ns)	Slack (ns)
DOUT<0>.Q to DOUT<10>.D	0.000	6.300	-6.300
DOUT<0>.Q to DOUT<11>.D	0.000	6.300	-6.300
DOUT<0>.Q to DOUT<12>.D	0.000	6.300	-6.300

Constraint: AUTO_TS_P2P

Description: MAXDELAY:FROM:PADS(*):TO:PADS(*):0.000 nS

Path	Requirement (ns)	Delay (ns)	Slack (ns)
CLK to RUN	0.000	17.000	-17.000
CLK to CARRY	0.000	12.500	-12.500
CLK to DOUT<0>	0.000	8.000	-8.000

Constraint: AUTO_TS_P2F

Description: MAXDELAY:FROM:PADS(*):TO:FFS(*):0.000 nS

Path	Requirement (ns)	Delay (ns)	Slack (ns)
RESET to READY.D	0.000	5.600	-5.600
RESET to START_S1.D	0.000	5.600	-5.600
RESET to START_S2.D	0.000	5.600	-5.600

Constraint: AUTO_TS_F2P

Description: MAXDELAY:FROM:FFS(*):TO:PADS(*):0.000 nS

Path	Requirement (ns)	Delay (ns)	Slack (ns)
DOUT<0>.Q to RUN	0.000	13.900	-13.900
DOUT<10>.Q to RUN	0.000	13.900	-13.900
DOUT<11>.Q to RUN	0.000	13.900	-13.900

Number of constraints not met: 4

Data Sheet Report

Maximum External Clock Speeds

Clock	fEXT (MHz)	Reason
START	227.273	Limited by Clock Pulse Width for START
STOP	227.273	Limited by Clock Pulse Width for STOP
CLK	158.730	Limited by Cycle Time for CLK

Setup/Hold Times for Clocks

Setup/Hold Times for Clock START

Source Pad	Setup to clk (edge)	Hold to clk (edge)

RESET	2.500	0.000

Setup/Hold Times for Clock STOP

Source Pad	Setup to clk (edge)	Hold to clk (edge)
RESET	2.500	0.000

Setup/Hold Times for Clock CLK

Source Pad	Setup to clk (edge)	Hold to clk (edge)
RESET	2.500	0.000

Clock to Pad Timing

Clock CLK to Pad

Destination Pad	Clock (edge) to Pad
RUN	17.000
CARRY	12.500
DOUT<0>	8.000
DOUT<10>	8.000
DOUT<11>	8.000
DOUT<12>	8.000
DOUT<13>	8.000
DOUT<14>	8.000
DOUT<15>	8.000
DOUT<1>	8.000
DOUT<2>	8.000
DOUT<3>	8.000
DOUT<4>	8.000
DOUT<5>	8.000
DOUT<6>	8.000
DOUT<7>	8.000
DOUT<8>	8.000
DOUT<9>	8.000
READY	8.000

Clock to Setup Times for Clocks

Clock to Setup for clock CLK

Source	Destination	Delay
DOUT<0>.Q	DOUT<10>.D	6.300
DOUT<0>.Q	DOUT<11>.D	6.300
DOUT<0>.Q	DOUT<12>.D	6.300
DOUT<0>.Q	DOUT<13>.D	6.300
DOUT<0>.Q	DOUT<14>.D	6.300
DOUT<0>.Q	DOUT<15>.D	6.300
DOUT<0>.Q	DOUT<1>.D	6.300
DOUT<0>.Q	DOUT<2>.D	6.300
DOUT<0>.Q	DOUT<3>.D	6.300
DOUT<0>.Q	DOUT<4>.D	6.300
DOUT<0>.Q	DOUT<5>.D	6.300
DOUT<0>.Q	DOUT<6>.D	6.300
DOUT<0>.Q	DOUT<7>.D	6.300
DOUT<0>.Q	DOUT<8>.D	6.300
DOUT<0>.Q	DOUT<9>.D	6.300
DOUT<10>.Q	DOUT<11>.D	6.300
DOUT<10>.Q	DOUT<12>.D	6.300
DOUT<10>.Q	DOUT<13>.D	6.300
DOUT<10>.Q	DOUT<14>.D	6.300
DOUT<10>.Q	DOUT<15>.D	6.300
DOUT<11>.Q	DOUT<12>.D	6.300
DOUT<11>.Q	DOUT<13>.D	6.300
DOUT<11>.Q	DOUT<14>.D	6.300
DOUT<11>.Q	DOUT<15>.D	6.300
DOUT<12>.Q	DOUT<13>.D	6.300
DOUT<12>.Q	DOUT<14>.D	6.300
DOUT<12>.Q	DOUT<15>.D	6.300
DOUT<13>.Q	DOUT<14>.D	6.300
DOUT<13>.Q	DOUT<15>.D	6.300
DOUT<14>.Q	DOUT<15>.D	6.300
DOUT<1>.Q	DOUT<10>.D	6.300
DOUT<1>.Q	DOUT<11>.D	6.300
DOUT<1>.Q	DOUT<12>.D	6.300
DOUT<1>.Q	DOUT<13>.D	6.300
DOUT<1>.Q	DOUT<14>.D	6.300
DOUT<1>.Q	DOUT<15>.D	6.300

DOUT<1>.Q	DOUT<2>.D	6.300
DOUT<1>.Q	DOUT<3>.D	6.300
DOUT<1>.Q	DOUT<4>.D	6.300
DOUT<1>.Q	DOUT<5>.D	6.300
DOUT<1>.Q	DOUT<6>.D	6.300
DOUT<1>.Q	DOUT<7>.D	6.300
DOUT<1>.Q	DOUT<8>.D	6.300
DOUT<1>.Q	DOUT<9>.D	6.300
DOUT<2>.Q	DOUT<10>.D	6.300
DOUT<2>.Q	DOUT<11>.D	6.300
DOUT<2>.Q	DOUT<12>.D	6.300
DOUT<2>.Q	DOUT<13>.D	6.300
DOUT<2>.Q	DOUT<14>.D	6.300
DOUT<2>.Q	DOUT<15>.D	6.300
DOUT<2>.Q	DOUT<3>.D	6.300
DOUT<2>.Q	DOUT<4>.D	6.300
DOUT<2>.Q	DOUT<5>.D	6.300
DOUT<2>.Q	DOUT<6>.D	6.300
DOUT<2>.Q	DOUT<7>.D	6.300
DOUT<2>.Q	DOUT<8>.D	6.300
DOUT<2>.Q	DOUT<9>.D	6.300
DOUT<3>.Q	DOUT<10>.D	6.300
DOUT<3>.Q	DOUT<11>.D	6.300
DOUT<3>.Q	DOUT<12>.D	6.300
DOUT<3>.Q	DOUT<13>.D	6.300
DOUT<3>.Q	DOUT<14>.D	6.300
DOUT<3>.Q	DOUT<15>.D	6.300
DOUT<3>.Q	DOUT<4>.D	6.300
DOUT<3>.Q	DOUT<5>.D	6.300
DOUT<3>.Q	DOUT<6>.D	6.300
DOUT<3>.Q	DOUT<7>.D	6.300
DOUT<3>.Q	DOUT<8>.D	6.300
DOUT<3>.Q	DOUT<9>.D	6.300
DOUT<4>.Q	DOUT<10>.D	6.300
DOUT<4>.Q	DOUT<11>.D	6.300
DOUT<4>.Q	DOUT<12>.D	6.300
DOUT<4>.Q	DOUT<13>.D	6.300
DOUT<4>.Q	DOUT<14>.D	6.300

DOUT<4>.Q	DOUT<15>.D	6.300
DOUT<4>.Q	DOUT<5>.D	6.300
DOUT<4>.Q	DOUT<6>.D	6.300
DOUT<4>.Q	DOUT<7>.D	6.300
DOUT<4>.Q	DOUT<8>.D	6.300
DOUT<4>.Q	DOUT<9>.D	6.300
DOUT<5>.Q	DOUT<10>.D	6.300
DOUT<5>.Q	DOUT<11>.D	6.300
DOUT<5>.Q	DOUT<12>.D	6.300
DOUT<5>.Q	DOUT<13>.D	6.300
DOUT<5>.Q	DOUT<14>.D	6.300
DOUT<5>.Q	DOUT<15>.D	6.300
DOUT<5>.Q	DOUT<6>.D	6.300
DOUT<5>.Q	DOUT<7>.D	6.300
DOUT<5>.Q	DOUT<8>.D	6.300
DOUT<5>.Q	DOUT<9>.D	6.300
DOUT<6>.Q	DOUT<10>.D	6.300
DOUT<6>.Q	DOUT<11>.D	6.300
DOUT<6>.Q	DOUT<12>.D	6.300
DOUT<6>.Q	DOUT<13>.D	6.300
DOUT<6>.Q	DOUT<14>.D	6.300
DOUT<6>.Q	DOUT<15>.D	6.300
DOUT<6>.Q	DOUT<7>.D	6.300
DOUT<6>.Q	DOUT<8>.D	6.300
DOUT<6>.Q	DOUT<9>.D	6.300
DOUT<7>.Q	DOUT<10>.D	6.300
DOUT<7>.Q	DOUT<11>.D	6.300
DOUT<7>.Q	DOUT<12>.D	6.300
DOUT<7>.Q	DOUT<13>.D	6.300
DOUT<7>.Q	DOUT<14>.D	6.300
DOUT<7>.Q	DOUT<15>.D	6.300
DOUT<7>.Q	DOUT<8>.D	6.300
DOUT<7>.Q	DOUT<9>.D	6.300
DOUT<8>.Q	DOUT<10>.D	6.300
DOUT<8>.Q	DOUT<11>.D	6.300
DOUT<8>.Q	DOUT<12>.D	6.300
DOUT<8>.Q	DOUT<13>.D	6.300
DOUT<8>.Q	DOUT<14>.D	6.300

DOUT<8>.Q	DOUT<15>.D	6.300
DOUT<8>.Q	DOUT<9>.D	6.300
DOUT<9>.Q	DOUT<10>.D	6.300
DOUT<9>.Q	DOUT<11>.D	6.300
DOUT<9>.Q	DOUT<12>.D	6.300
DOUT<9>.Q	DOUT<13>.D	6.300
DOUT<9>.Q	DOUT<14>.D	6.300
DOUT<9>.Q	DOUT<15>.D	6.300
READY.Q	DOUT<0>.D	6.300
READY.Q	DOUT<10>.D	6.300
READY.Q	DOUT<11>.D	6.300
READY.Q	DOUT<12>.D	6.300
READY.Q	DOUT<13>.D	6.300
READY.Q	DOUT<14>.D	6.300
READY.Q	DOUT<15>.D	6.300
READY.Q	DOUT<1>.D	6.300
READY.Q	DOUT<2>.D	6.300
READY.Q	DOUT<3>.D	6.300
READY.Q	DOUT<4>.D	6.300
READY.Q	DOUT<5>.D	6.300
READY.Q	DOUT<6>.D	6.300
READY.Q	DOUT<7>.D	6.300
READY.Q	DOUT<8>.D	6.300
READY.Q	DOUT<9>.D	6.300
START_S2.Q	XLXN_79.D	6.300
STOP_S2.Q	READY.D	6.300
XLXN_79.Q	DOUT<0>.D	6.300
XLXN_79.Q	DOUT<10>.D	6.300
XLXN_79.Q	DOUT<11>.D	6.300
XLXN_79.Q	DOUT<12>.D	6.300
XLXN_79.Q	DOUT<13>.D	6.300
XLXN_79.Q	DOUT<14>.D	6.300
XLXN_79.Q	DOUT<15>.D	6.300
XLXN_79.Q	DOUT<1>.D	6.300
XLXN_79.Q	DOUT<2>.D	6.300
XLXN_79.Q	DOUT<3>.D	6.300
XLXN_79.Q	DOUT<4>.D	6.300
XLXN_79.Q	DOUT<5>.D	6.300

XLXN_79.Q	DOUT<6>.D	6.300
XLXN_79.Q	DOUT<7>.D	6.300
XLXN_79.Q	DOUT<8>.D	6.300
XLXN_79.Q	DOUT<9>.D	6.300

Pad to Pad List

Source Pad	Destination Pad	Delay

Number of paths analyzed: 235
Number of Timing errors: 235
Analysis Completed: Sun Apr 10 20:47:49 2011
