```
cpldfit:  version O.40d                              Xilinx Inc.
                                  Fitter Report
Design Name: c3schem                                 Date: 12-17-2011, 10:25PM
Device Used: XC2C64A-7-VQ44
Fitting Status: Successful

*************************  Mapped Resource Summary  *************************

Macrocells     Product Terms    Function Block   Registers      Pins
Used/Tot       Used/Tot         Inps Used/Tot    Used/Tot       Used/Tot
24 /64   ( 37%) 22  /224  ( 10%) 37  /160  ( 23%) 22 /64   ( 34%) 27 /33   ( 82%)

** Function Block Resources **

Function Mcells   FB Inps  Pterms   IO       CTC      CTR      CTS      CTE
Block    Used/Tot Used/Tot Used/Tot Used/Tot Used/Tot Used/Tot Used/Tot Used/Tot
FB1       8/16      7/40     6/56     7/ 8    0/1      0/1      0/1      0/1
FB2       6/16      9/40     6/56     6/ 9    0/1      0/1      0/1      0/1
FB3       9/16     18/40     9/56     9/ 9*   0/1      0/1      0/1      0/1
FB4       1/16      3/40     1/56     1/ 7    0/1      0/1      0/1      0/1
          -----    -------  -------   -----    ---      ---      ---      ---
Total    24/64     37/160   22/224   23/33    0/4      0/4      0/4      0/4

CTC - Control Term Clock
CTR - Control Term Reset
CTS - Control Term Set
CTE - Control Term Output Enable

* - Resource is exhausted

** Global Control Resources **

GCK         GSR         GTS         DGE
Used/Tot    Used/Tot    Used/Tot    Used/Tot
3/3         1/1         0/4         0/0

Signal 'START' mapped onto global clock net GCK0.
Signal 'STOP' mapped onto global clock net GCK1.
Signal 'CLK' mapped onto global clock net GCK2.
Signal 'RESET' mapped onto global set/reset net GSR.

** Pin Resources **

Signal Type    Required     Mapped  |  Pin Type            Used    Total
------------------------------------|-------------------------------------
Input          :    0          0    |  I/O              :    19     25
Output         :   23         23    |  GCK/IO           :     3      3
Bidirectional  :    0          0    |  GTS/IO           :     4      4
GCK            :    3          3    |  GSR/IO           :     1      1
GTS            :    0          0    |
GSR            :    1          1    |
                  ----       ----
        Total     27         27

End of Mapped Resource Summary
*************************  Errors and Warnings  *************************

WARNING:Cpld - Unable to retrieve the path to the iSE Project Repository. Will
   use the default filename of 'c3schem.ise'.
```

□************************ Summary of Mapped Logic ************************

** 23 Outputs **

Signal Name	Total Pts	Total Inps	Bank	Loc	Pin No.	Pin Type	Pin Use	I/O STD	I/O Style
START_S1B	0	0	2	FB1_1	38	I/O	O	LVCMOS33	
STOP_S1B	0	0	2	FB1_2	37	I/O	O	LVCMOS33	
START_S2B	1	1	2	FB1_3	36	I/O	O	LVCMOS33	
START_S3B	1	1	2	FB1_9	34	GTS/I/O	O	LVCMOS33	
STOP_S3B	1	1	2	FB1_10	33	GTS/I/O	O	LVCMOS33	
DOUT<0>	1	2	2	FB1_11	32	GTS/I/O	O	LVCMOS33	
DOUT<1>	1	3	2	FB1_12	31	GTS/I/O	O	LVCMOS33	
DOUT<2>	1	4	1	FB2_1	39	I/O	O	LVCMOS33	
DOUT<3>	1	5	1	FB2_2	40	I/O	O	LVCMOS33	
DOUT<4>	1	6	1	FB2_5	41	I/O	O	LVCMOS33	
DOUT<5>	1	7	1	FB2_6	42	I/O	O	LVCMOS33	
DOUT<6>	1	8	1	FB2_12	2	I/O	O	LVCMOS33	
DOUT<7>	1	9	1	FB2_13	3	I/O	O	LVCMOS33	
DOUT<15>	1	17	2	FB3_1	29	I/O	O	LVCMOS33	
DOUT<14>	1	16	2	FB3_2	28	I/O	O	LVCMOS33	
DOUT<13>	1	15	2	FB3_3	27	I/O	O	LVCMOS33	
DOUT<12>	1	14	2	FB3_6	23	I/O	O	LVCMOS33	
DOUT<11>	1	13	2	FB3_10	22	I/O	O	LVCMOS33	
TC	1	16	2	FB3_11	21	I/O	O	LVCMOS33	
DOUT<10>	1	12	2	FB3_12	20	I/O	O	LVCMOS33	
DOUT<9>	1	11	2	FB3_14	19	I/O	O	LVCMOS33	
DOUT<8>	1	10	2	FB3_15	18	I/O	O	LVCMOS33	
CEO	1	3	1	FB4_1	5	I/O	O	LVCMOS33	

** 1 Buried Nodes **

Signal Name	Total Pts	Total Inps	Loc	Reg Use	Reg Init State
STOP_S2	1	1	FB1_16	DFF	RESET

** 4 Inputs **

Signal Name	Bank	Loc	Pin No.	Pin Type	Pin Use	I/O STD	I/O Style
RESET	2	FB1_13	30	GSR/I/O	GSR	LVCMOS33	S/KPR
START	1	FB2_7	43	GCK/I/O	GCK	LVCMOS33	S/KPR
STOP	1	FB2_8	44	GCK/I/O	GCK	LVCMOS33	S/KPR
CLK	1	FB2_10	1~	GCK/I/O	GCK	LVCMOS33	KPR

Legend:
Pin No. - ~   - User Assigned
I/O Style - OD   - OpenDrain
          - PU   - Pullup
          - KPR   - Keeper
          - S   - SchmittTrigger
          - DG   - DataGate
Reg Use   - LATCH - Transparent latch
          - DFF   - D-flip-flop
          - DEFF - D-flip-flop with clock enable
          - TFF   - T-flip-flop
          - TDFF - Dual-edge-triggered T-flip-flop
          - DDFF - Dual-edge-triggered flip-flop
          - DDEFF - Dual-edge-triggered flip-flop with clock enable
          /S (after any above flop/latch type) indicates initial state is Set

```
□□************************  Function Block Details  ************************
Legend:
Total Pt     - Total product terms used by the macrocell signal
Loc          - Location where logic was mapped in device
Pin Type/Use - I   - Input             GCK - Global clock
               O   - Output            GTS - Global Output Enable
              (b) - Buried macrocell   GSR - Global Set/Reset
              VRF - Vref
Pin No.      - ~   - User Assigned
□*********************************** FB1  ***********************************
This function block is part of I/O Bank number:                 2
Number of function block inputs used/remaining:                 7/33
Number of function block control terms used/remaining:          0/4
Number of PLA product terms used/remaining:                     6/50
Signal                          Total Loc     Pin  Pin     Pin   CTC CTR CTS CTE
Name                            Pt            No.  Type    Use
START_S1B                       0     FB1_1   38   I/O     O
STOP_S1B                        0     FB1_2   37   I/O     O
START_S2B                       1     FB1_3   36   I/O     O
(unused)                        0     FB1_4        (b)
(unused)                        0     FB1_5        (b)
(unused)                        0     FB1_6        (b)
(unused)                        0     FB1_7        (b)
(unused)                        0     FB1_8        (b)
START_S3B                       1     FB1_9   34   GTS/I/O O
STOP_S3B                        1     FB1_10  33   GTS/I/O O
DOUT<0>                         1     FB1_11  32   GTS/I/O O
DOUT<1>                         1     FB1_12  31   GTS/I/O O
(unused)                        0     FB1_13  30   GSR/I/O GSR
(unused)                        0     FB1_14       (b)
(unused)                        0     FB1_15       (b)
STOP_S2                         1     FB1_16       (b)     (b)

Signals Used by Logic in Function Block
  1: DOUT<0>            4: START_S3B          6: STOP_S2
  2: START_S1B          5: STOP_S1B           7: STOP_S3B
  3: START_S2B

Signal                      1         2         3         4 FB
Name              0----+----0----+----0----+----0----+----0 Inputs
START_S1B          ..................................... 0
STOP_S1B           ..................................... 0
START_S2B          .X................................... 1
START_S3B          ..X.................................. 1
STOP_S3B           .....X............................... 1
DOUT<0>            ...X..X.............................. 2
DOUT<1>            X..X..X.............................. 3
STOP_S2            ....X................................ 1
                  0----+----1----+----2----+----3----+----4
                       0         0         0         0
□*********************************** FB2  ***********************************
This function block is part of I/O Bank number:                 1
Number of function block inputs used/remaining:                 9/31
Number of function block control terms used/remaining:          0/4
Number of PLA product terms used/remaining:                     6/50
Signal                          Total Loc     Pin  Pin     Pin   CTC CTR CTS CTE
Name                            Pt            No.  Type    Use
DOUT<2>                         1     FB2_1   39   I/O     O
DOUT<3>                         1     FB2_2   40   I/O     O
(unused)                        0     FB2_3        (b)
```

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(unused)                        0     FB2_4         (b)
DOUT<4>                         1     FB2_5   41    I/O     O
DOUT<5>                         1     FB2_6   42    I/O     O
(unused)                        0     FB2_7   43    GCK/I/O GCK
(unused)                        0     FB2_8   44    GCK/I/O GCK
(unused)                        0     FB2_9         (b)
(unused)                        0     FB2_10  1     GCK/I/O GCK
(unused)                        0     FB2_11        (b)
DOUT<6>                         1     FB2_12  2     I/O     O
DOUT<7>                         1     FB2_13  3     I/O     O
(unused)                        0     FB2_14        (b)
(unused)                        0     FB2_15        (b)
(unused)                        0     FB2_16        (b)

Signals Used by Logic in Function Block
  1: DOUT<0>            4: DOUT<3>            7: DOUT<6>
  2: DOUT<1>            5: DOUT<4>            8: START_S3B
  3: DOUT<2>            6: DOUT<5>            9: STOP_S3B

Signal                      1         2         3         4 FB
Name              0----+----0----+----0----+----0----+----0 Inputs
DOUT<2>            XX.....XX............................... 4
DOUT<3>            XXX....XX............................... 5
DOUT<4>            XXXX...XX............................... 6
DOUT<5>            XXXXX..XX............................... 7
DOUT<6>            XXXXXX.XX............................... 8
DOUT<7>            XXXXXXXXX............................... 9
                  0----+----1----+----2----+----3----+----4
                            0         0         0         0
*********************************** FB3  ***********************************
This function block is part of I/O Bank number:                 2
Number of function block inputs used/remaining:                 18/22
Number of function block control terms used/remaining:          0/4
Number of PLA product terms used/remaining:                     9/47
Signal                          Total Loc     Pin  Pin     Pin   CTC CTR CTS CTE
Name                            Pt            No.  Type    Use
DOUT<15>                        1     FB3_1   29   I/O     O
DOUT<14>                        1     FB3_2   28   I/O     O
DOUT<13>                        1     FB3_3   27   I/O     O
(unused)                        0     FB3_4         (b)
(unused)                        0     FB3_5         (b)
DOUT<12>                        1     FB3_6   23   I/O     O
(unused)                        0     FB3_7         (b)
(unused)                        0     FB3_8         (b)
(unused)                        0     FB3_9         (b)
DOUT<11>                        1     FB3_10  22   I/O     O
TC                              1     FB3_11  21   I/O     O
DOUT<10>                        1     FB3_12  20   I/O     O
(unused)                        0     FB3_13        (b)
DOUT<9>                         1     FB3_14  19   I/O     O
DOUT<8>                         1     FB3_15  18   I/O     O
(unused)                        0     FB3_16        (b)

Signals Used by Logic in Function Block
  1: DOUT<0>            7: DOUT<15>           13: DOUT<6>
  2: DOUT<10>           8: DOUT<1>            14: DOUT<7>
  3: DOUT<11>           9: DOUT<2>            15: DOUT<8>
  4: DOUT<12>          10: DOUT<3>            16: DOUT<9>
  5: DOUT<13>          11: DOUT<4>            17: START_S3B
  6: DOUT<14>          12: DOUT<5>            18: STOP_S3B
```

```
Signal                      1         2         3         4 FB
Name              0----+----0----+----0----+----0----+----0 Inputs
DOUT<15>           XXXXXX.XXXXXXXXXX..................... 17
DOUT<14>           XXXXX..XXXXXXXXXX..................... 16
DOUT<13>           XXXX...XXXXXXXXXX..................... 15
DOUT<12>           XXX....XXXXXXXXXX..................... 14
DOUT<11>           XX.....XXXXXXXXXX..................... 13
TC                 XXXXXXXXXXXXXXXX...................... 16
DOUT<10>           X......XXXXXXXXXX..................... 12
DOUT<9>            X......XXXXXXXX.XX..................... 11
DOUT<8>            X......XXXXXXX..XX..................... 10
                  0----+----1----+----2----+----3----+----4
                       0         0         0         0
*********************************** FB4  ************************************
This function block is part of I/O Bank number:                 1
Number of function block inputs used/remaining:                 3/37
Number of function block control terms used/remaining:          0/4
Number of PLA product terms used/remaining:                     1/55
Signal                          Total Loc     Pin  Pin     Pin   CTC CTR CTS CTE
Name                            Pt            No.  Type    Use
CEO                             1     FB4_1   5    I/O     O
(unused)                        0     FB4_2   6    I/O
(unused)                        0     FB4_3         (b)
(unused)                        0     FB4_4         (b)
(unused)                        0     FB4_5         (b)
(unused)                        0     FB4_6         (b)
(unused)                        0     FB4_7   8    I/O
(unused)                        0     FB4_8         (b)
(unused)                        0     FB4_9         (b)
(unused)                        0     FB4_10        (b)
(unused)                        0     FB4_11  12   I/O
(unused)                        0     FB4_12        (b)
(unused)                        0     FB4_13  13   I/O
(unused)                        0     FB4_14  14   I/O
(unused)                        0     FB4_15  16   I/O
(unused)                        0     FB4_16        (b)

Signals Used by Logic in Function Block
  1: START_S3B          2: STOP_S3B           3: TC

Signal                      1         2         3         4 FB
Name              0----+----0----+----0----+----0----+----0 Inputs
CEO                XXX.................................... 3
                  0----+----1----+----2----+----3----+----4
                       0         0         0         0
*******************************  Equations  ********************************

********** Mapped Logic **********


CEO <= (START_S3B AND NOT STOP_S3B AND TC);

FTCPE_DOUT0: FTCPE port map (DOUT(0),DOUT_T(0),CLK,RESET,'0','1');
DOUT_T(0) <= (START_S3B AND NOT STOP_S3B);

FTCPE_DOUT1: FTCPE port map (DOUT(1),DOUT_T(1),CLK,RESET,'0','1');
DOUT_T(1) <= (START_S3B AND NOT STOP_S3B AND DOUT(0));

FTCPE_DOUT2: FTCPE port map (DOUT(2),DOUT_T(2),CLK,RESET,'0','1');
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DOUT_T(2) <= (START_S3B AND NOT STOP_S3B AND DOUT(0) AND DOUT(1));

FTCPE_DOUT3: FTCPE port map (DOUT(3),DOUT_T(3),CLK,RESET,'0','1');
DOUT_T(3) <= (START_S3B AND NOT STOP_S3B AND DOUT(0) AND DOUT(1) AND
        DOUT(2));

FTCPE_DOUT4: FTCPE port map (DOUT(4),DOUT_T(4),CLK,RESET,'0','1');
DOUT_T(4) <= (START_S3B AND NOT STOP_S3B AND DOUT(0) AND DOUT(1) AND
        DOUT(2) AND DOUT(3));

FTCPE_DOUT5: FTCPE port map (DOUT(5),DOUT_T(5),CLK,RESET,'0','1');
DOUT_T(5) <= (START_S3B AND NOT STOP_S3B AND DOUT(0) AND DOUT(1) AND
        DOUT(2) AND DOUT(3) AND DOUT(4));

FTCPE_DOUT6: FTCPE port map (DOUT(6),DOUT_T(6),CLK,RESET,'0','1');
DOUT_T(6) <= (START_S3B AND NOT STOP_S3B AND DOUT(0) AND DOUT(1) AND
        DOUT(2) AND DOUT(3) AND DOUT(4) AND DOUT(5));

FTCPE_DOUT7: FTCPE port map (DOUT(7),DOUT_T(7),CLK,RESET,'0','1');
DOUT_T(7) <= (START_S3B AND NOT STOP_S3B AND DOUT(0) AND DOUT(1) AND
        DOUT(2) AND DOUT(3) AND DOUT(4) AND DOUT(5) AND DOUT(6));

FTCPE_DOUT8: FTCPE port map (DOUT(8),DOUT_T(8),CLK,RESET,'0','1');
DOUT_T(8) <= (START_S3B AND NOT STOP_S3B AND DOUT(0) AND DOUT(1) AND
        DOUT(2) AND DOUT(3) AND DOUT(4) AND DOUT(5) AND DOUT(6) AND
        DOUT(7));

FTCPE_DOUT9: FTCPE port map (DOUT(9),DOUT_T(9),CLK,RESET,'0','1');
DOUT_T(9) <= (START_S3B AND NOT STOP_S3B AND DOUT(0) AND DOUT(1) AND
        DOUT(2) AND DOUT(3) AND DOUT(4) AND DOUT(5) AND DOUT(6) AND
        DOUT(7) AND DOUT(8));

FTCPE_DOUT10: FTCPE port map (DOUT(10),DOUT_T(10),CLK,RESET,'0','1');
DOUT_T(10) <= (START_S3B AND NOT STOP_S3B AND DOUT(0) AND DOUT(1) AND
        DOUT(2) AND DOUT(3) AND DOUT(4) AND DOUT(5) AND DOUT(6) AND
        DOUT(7) AND DOUT(8) AND DOUT(9));

FTCPE_DOUT11: FTCPE port map (DOUT(11),DOUT_T(11),CLK,RESET,'0','1');
DOUT_T(11) <= (START_S3B AND NOT STOP_S3B AND DOUT(0) AND DOUT(1) AND
        DOUT(2) AND DOUT(3) AND DOUT(4) AND DOUT(5) AND DOUT(6) AND
        DOUT(7) AND DOUT(8) AND DOUT(9) AND DOUT(10));

FTCPE_DOUT12: FTCPE port map (DOUT(12),DOUT_T(12),CLK,RESET,'0','1');
DOUT_T(12) <= (START_S3B AND NOT STOP_S3B AND DOUT(0) AND DOUT(1) AND
        DOUT(2) AND DOUT(3) AND DOUT(4) AND DOUT(5) AND DOUT(6) AND
        DOUT(7) AND DOUT(8) AND DOUT(9) AND DOUT(10) AND DOUT(11));

FTCPE_DOUT13: FTCPE port map (DOUT(13),DOUT_T(13),CLK,RESET,'0','1');
DOUT_T(13) <= (START_S3B AND NOT STOP_S3B AND DOUT(0) AND DOUT(1) AND
        DOUT(2) AND DOUT(3) AND DOUT(4) AND DOUT(5) AND DOUT(6) AND
        DOUT(7) AND DOUT(8) AND DOUT(9) AND DOUT(10) AND DOUT(11) AND
        DOUT(12));

FTCPE_DOUT14: FTCPE port map (DOUT(14),DOUT_T(14),CLK,RESET,'0','1');
DOUT_T(14) <= (START_S3B AND NOT STOP_S3B AND DOUT(0) AND DOUT(1) AND
        DOUT(2) AND DOUT(3) AND DOUT(4) AND DOUT(5) AND DOUT(6) AND
        DOUT(7) AND DOUT(8) AND DOUT(9) AND DOUT(10) AND DOUT(11) AND
        DOUT(12) AND DOUT(13));

FTCPE_DOUT15: FTCPE port map (DOUT(15),DOUT_T(15),CLK,RESET,'0','1');
```

```
DOUT_T(15) <= (START_S3B AND NOT STOP_S3B AND DOUT(0) AND DOUT(1) AND
        DOUT(2) AND DOUT(3) AND DOUT(4) AND DOUT(5) AND DOUT(6) AND
        DOUT(7) AND DOUT(8) AND DOUT(9) AND DOUT(10) AND DOUT(11) AND
        DOUT(12) AND DOUT(13) AND DOUT(14));

FDCPE_START_S1B: FDCPE port map (START_S1B,NOT '0',START,RESET,'0','1');

FDCPE_START_S2B: FDCPE port map (START_S2B,START_S1B,CLK,RESET,'0','1');

FDCPE_START_S3B: FDCPE port map (START_S3B,START_S2B,CLK,RESET,'0','1');

FDCPE_STOP_S1B: FDCPE port map (STOP_S1B,NOT '0',STOP,RESET,'0','1');

FDCPE_STOP_S2: FDCPE port map (STOP_S2,STOP_S1B,CLK,RESET,'0','1');

FDCPE_STOP_S3B: FDCPE port map (STOP_S3B,STOP_S2,CLK,RESET,'0','1');


TC <= (DOUT(0) AND DOUT(1) AND DOUT(2) AND DOUT(3) AND
        DOUT(4) AND DOUT(5) AND DOUT(6) AND DOUT(7) AND DOUT(8) AND
        DOUT(9) AND DOUT(10) AND DOUT(11) AND DOUT(12) AND DOUT(13) AND
        DOUT(14) AND DOUT(15));


Register Legend:
 FDCPE (Q,D,C,CLR,PRE,CE);
 FDDCPE (Q,D,C,CLR,PRE,CE);
 FTCPE (Q,D,C,CLR,PRE,CE);
 FTDCPE (Q,D,C,CLR,PRE,CE);
 LDCP  (Q,D,G,CLR,PRE);

□****************************  Device Pin Out *****************************

Device : XC2C64A-7-VQ44


   --------------------------------
  /44 43 42 41 40 39 38 37 36 35 34 \
 | 1                                33 |
 | 2                                32 |
 | 3                                31 |
 | 4                                30 |
 | 5          XC2C64A-7-VQ44        29 |
 | 6                                28 |
 | 7                                27 |
 | 8                                26 |
 | 9                                25 |
 | 10                               24 |
 | 11                               23 |
 \ 12 13 14 15 16 17 18 19 20 21 22 /
   --------------------------------


Pin Signal                          Pin Signal
No. Name                            No. Name
  1 CLK                               23 DOUT<12>
  2 DOUT<6>                           24 TDO
  3 DOUT<7>                           25 GND
  4 GND                               26 VCCIO-3.3
  5 CEO                               27 DOUT<13>
```

```
  6 KPR                                28 DOUT<14>
  7 VCCIO-3.3                          29 DOUT<15>
  8 KPR                                30 RESET
  9 TDI                                31 DOUT<1>
 10 TMS                                32 DOUT<0>
 11 TCK                                33 STOP_S3B
 12 KPR                                34 START_S3B
 13 KPR                                35 VCCAUX
 14 KPR                                36 START_S2B
 15 VCC                                37 STOP_S1B
 16 KPR                                38 START_S1B
 17 GND                                39 DOUT<2>
 18 DOUT<8>                            40 DOUT<3>
 19 DOUT<9>                            41 DOUT<4>
 20 DOUT<10>                           42 DOUT<5>
 21 TC                                 43 START
 22 DOUT<11>                           44 STOP


Legend :  NC  = Not Connected, unbonded pin
         PGND  = Unused I/O configured as additional Ground pin
          KPR  = Unused I/O with weak keeper (leave unconnected)
          WPU  = Unused I/O with weak pull up (leave unconnected)
          TIE  = Unused I/O floating -- must tie to VCC, GND or other signal
          VCC  = Dedicated Power Pin
       VCCAUX  = Power supply for JTAG pins
    VCCIO-3.3  = I/O supply voltage for LVTTL, LVCMOS33, SSTL3_I
    VCCIO-2.5  = I/O supply voltage for LVCMOS25, SSTL2_I
    VCCIO-1.8  = I/O supply voltage for LVCMOS18
    VCCIO-1.5  = I/O supply voltage for LVCMOS15, HSTL_I
         VREF  = Reference voltage for indicated input standard
        *VREF  = Reference voltage pin selected by software
          GND  = Dedicated Ground Pin
          TDI  = Test Data In, JTAG pin
          TDO  = Test Data Out, JTAG pin
          TCK  = Test Clock, JTAG pin
          TMS  = Test Mode Select, JTAG pin
   PROHIBITED  = User reserved pin
□**************************  Compiler Options  ***************************

Following is a list of all global compiler options used by the fitter run.

Device(s) Specified                          : xc2c64a-7-VQ44
Optimization Method                          : DENSITY
Multi-Level Logic Optimization               : ON
Ignore Timing Specifications                 : OFF
Default Register Power Up Value              : LOW
Keep User Location Constraints               : ON
What-You-See-Is-What-You-Get                 : OFF
Exhaustive Fitting                           : OFF
Keep Unused Inputs                           : OFF
Slew Rate                                    : FAST
Set Unused I/O Pin Termination               : KEEPER
Global Clock Optimization                    : ON
Global Set/Reset Optimization                : ON
Global Ouput Enable Optimization             : ON
Enable Input Registers                       : ON
Function Block Fan-in Limit                  : 38
Use DATA_GATE Attribute                      : ON
Set Tristate Outputs to Termination Mode     : KEEPER
```

```
Default Voltage Standard for All Outputs    : LVCMOS18
Input Limit                                 : 32
Pterm Limit                                 : 28
```

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